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initiates the refresh of the memory cells, is generated when the counter has incremented to one of a first counter stage in the full density mode and a counter stage two stages beyond the first counter stage in the half density mode. Circuitry is also provided for ignoring some auto-refresh commands applied to the SDRAM in the half density mode so that the memory cells are also refreshed less frequently in the auto-refresh mode. The SDRAM also includes circuitry for remapping one of the row address bits for use as a column address bit in the half density mode so that the SDRAM can interface with system adapted for conventional dual mode SDRAMs.

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#### REMARKS

Claims 17, 18, 30, 31, 39, 40, 44 and 45 have been presented for examination. Claims 31 and 40 have been rejected under 35 U.S.C. §112 as being indefinite. Additionally, claim 44 has been objected to because of the presence of a duplicate word, and the abstract and specification have been objected to for not accurately describing the subject matter shown in the Figures.

Applicant is hereby amending claims 31 and 40 to overcome the Section 112 rejections, and amending claim 44, the specification and the abstract to obviate the objections to the claims, specification and abstract, respectively.

Insofar as the specification, abstract and claims 17, 18, 30, 31, 39, 40, 44 and 45 are now in proper form, favorable consideration and a Notice of Allowance are earnestly solicited.

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Attached hereto is a marked-up version of the changes made to the specification, claims and abstract by the current amendment. The attached page is captioned "Version with Markings to Show Changes Made".

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Paragraph beginning at line 26 of page 16 has been amended as follows:

As mentioned above, the column address buffers 34 are designed to remap one of the row address to a column address so that the SDRAM 20 is plug compatible with SDRAMs adapted to receive row addresses for M rows and column addresses for N/2 columns. With reference to Figure 4, a portion of the column address buffers 34 includes a latch 260 that receives ten column address bits CA0-CA9. The column address buffer 260 latches the address bits responsive to an active low column address strobe read/write command, as is well known in the art. The nine low order address bits CA0-CA8 are applied to the column decoder 56 (Figure 1) in a conventional manner. However, the most significant column address bit CA9 is applied to a pass gate 264. Another pass gate 266 receives the output of a latch 270 that stores the most significant row address bit [RA0]RA11 responsive to an activate command. The pass gates 264, 266 are controlled by the active low density control signal HD\* directly and through an inverter 274. When the HD\* signal is inactive high indicative of the full density mode of operation, the pass gate 264 is enabled and the pass gate 266 is disabled so that the latched most significant column address bit CA9 is applied to the column decoder 56 along with the lower order column address bits CA0-CA8. Thus, in the full density mode, the column address buffers 34 operate in a conventional manner. When the HD\* signal is active low indicative of the half density mode of operation, the pass gate 264 is disabled and the pass gate 266 is enabled so that the most significant [column address bit CA9]row address bit RA11 is applied by the pass gate 266. As is well known in the art, the row addresses are received prior to the column addresses, and they are latched into the SDRAM 20 responsive to the activate command. In the column address buffers 34 showed in Figure 4, the most significant row address bit RA0 is stored in the latch 270 responsive to the activate command and is then selected by the pass gate 266 for use as the most significant column address bit CA9. In this manner, the most significant row address bit [RA0]RA11 is remapped to be the most significant column address bit CA9 thereby making the SDRAM 20 with a capacity of M/2 rows \* N columns plug compatible with SDRAMs adapted to receive row addresses for M rows and column addresses for N/2 columns.

In the Claims:

Claims 31, 40 and 44 have been amended as follows:

31. (Amended) The dynamic random access memory of claim 30 wherein the selector comprises:

a first pass gate coupled between an output of the [first]column address latch and an address output terminal;

a second pass gate coupled between an output of the [second]remapping latch and the address output terminal; and

a control circuit for enabling the first pass gate and disabling the second pass gate or disabling the first pass gate and enabling the second pass gate.

40. (Amended) The computer system of claim 39 wherein the selector comprises:

a first pass gate coupled between an output of the [first]column address latch and an address output terminal;

a second pass gate coupled between an output of the [second]remapping latch and the address output terminal; and

a control circuit for enabling the first pass gate and disabling the second pass gate or disabling the first pass gate and enabling the second pass gate.

44. (Amended) A method of addressing a dynamic random access memory ("DRAM") having a full density operating mode and a reduced density operating mode, the method comprising:

determining the operating mode of the DRAM;

storing a specific row address bit responsive to a row address strobe signal;

storing a first set of column address bits and a specific column address bit responsive to a column address strobe signal; and

in the full density operating mode, selecting the first set of column address bits and the specific column address bit that were stored responsive to the column address strobe signal;

in the reduced density operating mode, selecting the first set of column address bits that were stored responsive to the column address strobe signal and the specific row address bit that was stored responsive to the row address strobe signal; and

addressing a column of the [the] DRAM using the selected address bits.

In the Abstract:

The abstract beginning on page 40 has been amended as follows:

A dual mode, full density/half density SDRAM includes a refresh controller specifically adapted to refresh memory cells of the SDRAM in the half density mode at a rate that is significantly slower than the rate at which the memory cells are refreshed in the full density mode. In the [full]half density mode, the refresh controller increments a counter at a rate that is half the rate the counter is incremented in the full density mode. A refresh trigger pulse, which initiates the refresh of the memory cells, is generated when the counter has incremented to one of a first counter stage in the full density mode and a counter stage two stages beyond the first counter stage in the half density mode. Circuitry is also provided for ignoring some auto-refresh commands applied to the SDRAM in the half density mode so that the memory cells are also refreshed less frequently in the auto-refresh mode. The SDRAM also includes circuitry for remapping one of the row address bits for use as a column address bit in the half density mode so that the SDRAM can interface with system adapted for conventional dual mode SDRAMs.

